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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/712,711
Filing Date: November 12, 2003
Appellant(s): MUKUND ET AL.

Jayarthi Minisadram
For Appellant

EXAMINER'S ANSWER

This is in response to due to a remand from the Board of Patent Appeals and Interferences on 05/07/09. In response to the remand, Appellants filed an appeal brief on 07/24/09 appealing from the Office action mailed 11/29/06. No new grounds of rejection made in this answer. The Examiner's Answer mailed on 11/16/07 has been vacated.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

2002/0152061A1	SHIMOGORI et al.	10-2002
5,815,714	SHRIDHAR et al.	9-1998

(9) Grounds of Rejection

The following grounds of rejection are applicable to the appealed claims:

Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimogori et al. (U.S. Patent Application No. 2002/0152061A1) **in view of Shridhar et al. (U.S. Patent No. 5,815,714).**

As per claim 1, Shimogori is directed to a method for simulating a chip circuit **([0053])**, comprising: defining a library of components for a processor **([0082]-[0083])**; defining interconnections for a set of pipelined processors including the processor **([0047])**, the interconnections defined by analyzing the architectural representation of adjacent processors **([0047]-[0048])**; generating a processor circuit by combining the library of components and the interconnections for the set of pipelined processors **([0083])**; generating a code representation of a model of the set of pipelined processors **([0058])**; and comparing signals generated by the code representation to signals generated by the processor circuit **([0062])**, wherein if the comparison of the signals is unacceptable, the method includes, identifying a cause of the unacceptable comparison of the signals at a block level of the processor circuit **([0090])** but fails to explicitly disclose generating output for display to identify a cause of the unacceptable comparison of the signals at a block level of the processor circuit.

Shridhar teaches inserting a print command to determine the signal level location of an error **(column 4, lines 40-42)**. Shimogori and Shridhar are analogous art because they are from the same field of endeavor, testing and debugging code. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the chip circuit simulation method of Shimogori with the debugging print commands of Shridhar in order to provide convenient means for modifying the underlying source code as required **(Shridhar, column 3, lines 44-47)**.

As per claim 2, the combination of Shimogori and Shridhar already discloses the method of claim 1, wherein the library of components is included as register transfer logic (RTL) **(Shimogori, [0053])**.

As per claim 3, the combination of Shimogori and Shridhar already discloses the method of claim 1, wherein the interconnections for the set of pipelined processors is included in a structural netlist **(Shimogori, [0099])**.

As per claim 4, the combination of Shimogori and Shridhar already discloses the method of claim 1, wherein the set of pipelined processors are configured to manipulate layers of a header of a data packet in stages **(Shimogori, [0068])**.

As per claim 5, the combination of Shimogori and Shridhar already discloses the method of claim 1, wherein the method operation of identifying a cause of the unacceptable comparison of the signals at a block level of the processor circuit includes, inserting a patch into the code representation to identify a signal level location for the unacceptable comparison of the signals **(Shimogori, [0091])**.

As per claim 6, the combination of Shimogori and Shridhar already discloses a method for debugging a processor circuit, comprising: identifying a block level location having an error from a first simulation **(Shimogori, [0090])**; inserting a patch into a thread specific to the block level location of the error **(Shimogori, [0091])**; executing the simulation to determine a signal level location of the error through information generated by the patch **(Shimogori, [0091])**; and correcting a code representation of a processor associated with the error **(Shimogori, [0093])**.

As per claim 7, the combination of Shimogori and Shridhar already discloses the method of claim 6, wherein the patch is a print command **(Shridhar, column 4, lines 40-42)**.

As per claim 8, the combination of Shimogori and Shridhar already discloses the method of claim 6, wherein the method operation of executing the simulation to determine a signal level location through information generated by the patch includes, triggering a print statement indicating the signal level location of the error **(Shridhar, column 4, lines 40-42)**.

As per claim 9, Shimogori is directed to an apparatus for simulating a chip circuit **([0053])**, comprising: a server in which a simulation program logic is stored, the server configured to execute the

simulation program logic **([0018])**, wherein the simulation program logic includes: logic for generating a processor circuit by combining a library of components and defined interconnections for a set of pipelined processors **([0082]-[0083], [0047])** the interconnections defined by analyzing the architectural representation of adjacent processors **([0047]-[0048])**; logic for generating a code representation of a model of the processor **([0058])**; and logic for comparing signals generated by the code representation to signals generated by the processor circuit **([0062])**, wherein if the comparison of the signals is unacceptable, the logic for comparing signals includes, logic for identifying a cause of the unacceptable comparison of the signals at a block level of the code representation **([0090])** but fails to explicitly disclose generating output for display to identify a cause of the unacceptable comparison of the signals at a block level of the code representation.

Shridhar teaches inserting a print command to determine the signal level location of an error **(column 4, lines 40-42)**. Shimogori and Shridhar are analogous art because they are from the same field of endeavor, testing and debugging code. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the chip circuit simulation method of Shimogori with the debugging print commands of Shridhar in order to provide convenient means for modifying the underlying source code as required **(Shridhar, column 3, lines 44-47)**.

As per claim 10, the combination of Shimogori and Shridhar already discloses the apparatus of claim 9, wherein logic for identifying a cause of the unacceptable comparison of the signals at a block level of the processor circuit includes, logic for inserting a patch into the code representation to identify a signal level location for the unacceptable comparison of the signals **(Shimogori, [0091])**.

As per claim 11, the combination of Shimogori and Shridhar already discloses the apparatus of claim 9, wherein the library of components is included as register transfer logic (RTL) **(Shimogori, [0053])**.

As per claim 12, the combination of Shimogori and Shridhar already discloses the apparatus of claim 9, wherein the interconnections for the set of pipelined processors is included in a structural netlist **(Shimogori, [0099])**.

As per claim 13, the combination of Shimogori and Shridhar already discloses the apparatus of claim 10, wherein the patch includes logic for executing a print statement **(Shridhar, column 4, lines 40-42)**.

As per claim 14, the combination of Shimogori and Shridhar already discloses the apparatus of claim 9, wherein each logic component is one of hardware and software **(Shimogori, [0101])**.

As per claim 15, Shimogori is directed to a computer readable medium **([0101])** in which program instructions are stored, the program instructions when read by a server of a computing system **([0018])**, cause the server to perform a method for simulating a model of a chip circuit, the method comprising: defining a library of components for a processor **([0082]-[0083])**; defining interconnections for a set of pipelined processors including the processor **([0047])**, the interconnections defined by analyzing the architectural representation of adjacent processors; generating a processor circuit by combining the library of components and the interconnections for the set of pipelined processors **([0083])**; generating a code representation of a model of the set of pipelined processors **([0058])**; and comparing signals generated by the code representation to signals generated by the processor circuit **([0062])**, wherein if the comparison of the signals is unacceptable, the method includes, identifying a cause of the unacceptable comparison of the signals at a block level of the processor circuit **([0090])** but fails to explicitly disclose generating output for display to identify a cause of the unacceptable comparison of the signals at a block level of the processor circuit.

Shridhar teaches inserting a print command to determine the signal level location of an error **(column 4, lines 40-42)**. Shimogori and Shridhar are analogous art because they are from the same field of endeavor, testing and debugging code. It would have been obvious to one of ordinary skill in the art at

the time of the invention to combine the chip circuit simulation method of Shimogori with the debugging print commands of Shridhar in order to provide convenient means for modifying the underlying source code as required **(Shridhar, column 3, lines 44-47)**.

As per claim 16, the combination of Shimogori and Shridhar already discloses the computer readable medium of claim 15, wherein the library of components is included as register transfer logic (RTL) **(Shimogori, [0053])**.

As per claim 17, the combination of Shimogori and Shridhar already discloses the computer readable medium of claim 15, wherein the interconnections for the set of pipelined processors are included in a structural netlist **(Shimogori, [0099])**.

As per claim 18, the combination of Shimogori and Shridhar already discloses the computer readable medium of claim 15, wherein the set of pipelined processors are configured to manipulate layers of a header of a data packet in stages **(Shimogori, [0068])**.

As per claim 19, the combination of Shimogori and Shridhar already discloses the computer readable medium of claim 15, wherein identifying a cause of the unacceptable comparison of the signals at a block level of the processor circuit includes, program instructions for inserting a patch into the code representation to identify a signal level location for the unacceptable comparison of the signals **(Shimogori, [0091])**.

(10) Response to Argument

Appellants argue a variety of reasons in support of their position that expressly claimed limitations are not disclosed by the cited prior art.

A) Shimogori teaches block level processing.

On pages 5-6 of the Appeal Brief, the Appellants argue that Shimogori does not disclose block level processing. However, the claims fail to provide a definition of block level processing, the specification of the instant application fails to provide a definition of block level processing, and Appellants have provided no detailed explanation on what they believe to be the definition of block level processing in any of their arguments during the course of the prosecution of the instant application. The Appellants have only provided mere allegation of patentability of block level processing without specifically pointing out how the language of the claims patentably distinguishes them from the references.

The Examiner has interpreted block level representation (and processing) as representation at the device level wherein there are blocks of code, or objects which may be converted into hardware **(Shimogori, [0095]-[0096])**. The interpretation of block level in Shimogori agrees with the implied definition of block level in the specification of the instant application as stated in paragraph **[0006]** in the Background of the Invention, "Chip 100 includes blocks A-F, where block A is represented twice. For example, block A could be a memory that is replicated." Although Shimogori does not explicitly state "block level" it operates at a block level as interpreted by the Examiner. Thus, by identifying a portion of code that can be speeded up wherein blocks of code represent devices such a memory, Shimogori identifies at a block level the cause of the unacceptable comparison of the signals and inserts a patch into a thread specific of the block level location of the error (**[0090]**).

B) Shimogori teaches identifying a cause of unacceptable comparison of signals at a block level.

On page 6 of the Appeal Brief, in regards to claim 1, the Appellants argue that Shimogori does not disclose identifying a location of a cause of the unacceptable comparison of the signals or an "error" and that the "error" of Shimogori is "not actually an error". However, nowhere does claim 1 recite an "error", only that the method of claim 1 identifies the location of a "cause of the unacceptable comparison of the signals at the block level". It is noted that the features upon which applicant relies (i.e., error) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). A cause of an unacceptable comparison of signals includes a signal output which is delayed and must be sped up because the number of clock cycles a particular piece of code takes is too long and merely "a defect in a chip that when left undetected can cause drastic consequences during the operation of the chip, i.e. the chip will not function" as alleged by the Appellants on page 6 of the Appeal Brief. Thus by identifying portions of software that must be sped up, Shimogori discloses identifying a location of a cause of the unacceptable comparison of the signals at the block level (**[0090]**).

However, claim 6 does recite the identification of an error, but Shimogori still discloses said claimed error. A triggering signal generated by a particular piece of code when the code takes too many cycles to run will cause a chip not to function properly, thus becomes a defect of the chip which will output erroneous signals.

C) Shimogori teaches a patch inserted into a thread specific to the block level location of an error.

On page 7 of the Appeal Brief, in regards to claim 6, the Appellants argue that the patch of Shimogori does not render the patch of the claimed invention obvious. The Appellants argue that the

purpose of the patch of Shimogori (curing an error) is not the same as the purpose of the patch of the claimed invention (further defining the location of an error). However, Appellants are arguing intended use which is not given patentable weight. While the limitation "inserting a patch into a thread specific to the block level location of the error" is given patentable weight and is disclosed by Shimogori in paragraph **[0091]** the limitation of intended use "to determine a signal level location of the error through information generated by the patch" is not.

D) *Shimogori teaches running a second simulation for further identifying the signal level location of the error.*

On page 7 of the Appeal Brief, in regards to claim 6, the Appellants argue that Shimogori does not suggest "executing the simulation (again) to determine a signal level location of the error through information generated by the patch" which is directed towards the intended use of executing the simulation. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. Shimogori clearly teaches executing the simulation a second time in paragraphs **[0031]** (*"Also as a third stage, the special-purpose instruction library may be converted into TRL before another ISS simulation is performed"*) and **[0091]** (*"a simulation step (step 126) may be inserted at this stage, though such simulation may be skipped if not required, with only the simulation in the latter stage of the processing being performed"*). The second simulation is capable of performing the intended use and as such renders claim 6 obvious.

(11) Related Proceedings Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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